Deere Co., 383 U.S. 1 (1966) and *United States v. Adams*, 383 U.S. 39 (1966)). "As adapted to *ex parte* procedure, *Graham* is interpreted as continuing to place the 'burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103'." *In re Piasecki*, 745 F.2d 1468 (Fed. Cir. 1984) (citing *In re Warner*, 379 F.2d at 1016).

"The prima facie case is a procedural tool which, as used in patent examination (as by courts in general), means not only that the evidence of the prior art would reasonably allow the conclusion the examiner seeks, but also that the prior art compels such a conclusion if the applicant produces no evidence or argument to rebut it." *In re Spada*, 911 F.2d 705, 708 n.3 (Fed. Cir. 1990).

The applicant respectfully submits the Examiner has failed to meet the burden of proof required to establish a prima facie case of anticipation. Section 2131 of the Manual of Patent Examiner's Procedure provides:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053, (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim . . . . *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

With respect to independent Claim 1, the Examiner has failed to provide a prima facie case of anticipation because the Examiner failed to provide any teaching in Barbier of "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 1. Barbier appears to merely teach "The system enables the making of half-tones by using the control circuits of the matrix which are not usually designed for this purpose

while producing no flicker effect. The system has a memory image with N (greater than or equal or 2) memory planes to store therein light information relating to each pixel in an N-bit word. The planes are read sequentially and thus make N-1 half-tones. In the simplest case (n=2), two planes are used and a first image is produced where any pixel is formed by a first bit, extracted from a first plane, and is preceded and followed, in rows as well as in columns, by a pixel formed by a first bit extraced [sic] from the other plane. The addressing is then determined to produce a second image by extracting, in reverse and respectively by each pixel, the second luminance bit in the other memory plane not used for the first image."

With respect to Claim 2, the Examiner stated, "Barbier et al teaches a luminance state presenting a first interval 1/FO around a mean value b+ (first predetermined amount, col. 5, lines 10-11)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the Examiner has failed to address the further limitation, "wherein the value of said first predetermined amount is selected as a function of said first pixel value" of Claim 2.

With respect to Claim 3, the Examiner stated, "Barbier et al teaches a luminance state presenting a first interval 1/FO around a mean value b+ (first offset value b+ is greater than a first pixel value b, col. 5, lines 9-12)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the Examiner has failed to address the further limitation, "wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed" of Claim 3.

With respect to Claim 4, the Examiner stated, "Barbier et al teaches the pixels value a and b extracting from a plurality of weight-bit plane A1, A2 and B1, B2 (col. 3, lines 52-59)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the Examiner has failed to address the further limitation, "said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame" of Claim 4.

With respect to independent Claim 6, the Examiner has failed to provide a prima facie case of anticipation because the Examiner failed to provide any teaching in Barbier of "a logic

circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 6.

The Examiner stated, "Barbier et al teaches a system of displaying digital image which includes a graphic processor 2 (logic circuit) controlling/offsetting by a processor 1 (figure 1, col. 3, lines 1-3), a luminance state presenting a first interval 1/FO around a mean value b+ (first offset value) and a second interval 1/FO around a mean value b- (second offset value, col. 5, lines 9-12), a display screen 11 (col. 3, lines 4-6) displays the two different binary states of luminance a and b, a is the luminance level of a lit pixel (a first offset pixel value display frame), and b is the luminance level of an off pixel (the opposite/second offset pixel value display frame), the making of the semi-luminance (a+b)/2 (average of a displayed first offset pixel value and a second offset pixel value, figure 3 and 4, col. 5, lines 36-40)."

The applicant submits the teachings of Barbier simply do not support the Examiner's transformation of Barbier's display of multiple bit planes, into the system described by applicant's Claim 6. The Examiner has failed to point to any teaching in Barbier of "offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value" recited by Claim 6.

With respect to Claim 7, the Examiner stated, "Barbier et al teaches a graphic processor 2 controlling a luminance state presenting a first interval 1/FO around a mean value b+ (first predetermined amount, col. 5, lines 10-11)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the Examiner has failed to address the further limitation, "the value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value" of Claim 7.

With respect to Claim 8, the Examiner stated, "Barbier et al teaches a graphic processor 2 controlling a luminance state presenting a first interval 1/FO around a mean value b+ (first offset

value b+ is greater than a first pixel value b, col. 5, lines 9-12)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the Examiner has failed to address the further limitation, "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed" of Claim 8.

With respect to Claim 9, the Examiner stated, "Barbier et al teaches a graphic processor 2 controlling the pixels value a and b extracting from a plurality of weight-bit plane A1, B1 and A2, B2 (col. 3, lines 52-59)." The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the Examiner has failed to address the further limitation, "said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame" of Claim 9.

In view of the remarks presented herewith, it is believed that the claims currently in the application, Claims 1-10, accord with the requirements of 35 U.S.C. § 112 and are allowable over the prior art of record. Therefore, it is urged that Claims 1-10 are in condition for allowance. Reconsideration of the present application is respectfully requested.

Respectfully submitted,

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